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Class	9th	Chapter	03
Subject	Computer Science	Board	Punjab

CHAPTER 3: DIGITAL SYSTEMS AND LOGIC DESIGN (EXERCISE SOLUTION)

Multiple-Choice Questions (MCQs)

1. Which of the following Boolean expressions represents the OR operation?

a) $A \cdot B$ b) $A + B$ c) $\bar{A}$ d) $A \oplus B$

Answer: b) $A + B$

2. What is the dual of the Boolean expression $A \cdot 0 = 0$?

a) $A + 1 = 1$ b) $A + 0 = A$ c) $A \cdot 1 = A$ d) $A \cdot 0 = 0$

Answer: a) $A + 1 = 1$

3. Which logic gate outputs true only if both inputs are true?

a) OR gate b) AND gate c) XOR gate d) NOT gate

Answer: b) AND gate

4. In a half-adder circuit, the carry is generated by which operation?

a) XOR operation b) AND operation c) OR operation d) NOT operation

Answer: b) AND operation

5. What is the decimal equivalent of the binary number 1101?

a) 11 b) 12 c) 13 d) 14

Answer: c) 13

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Short Questions

1. Define a Boolean function and give an example.

Answer: A Boolean function is an algebraic expression formed using binary variables, binary operators (AND ·, OR +, NOT $\overline{X}$), and logical constants (0 and 1). It outputs a single binary value (0 or 1) based on its input variables.

Example: $F(A, B) = A \cdot B + \bar{A}$.

2. What is the significance of the truth table in digital logic?

Answer: A truth table provides a complete tabular representation listing all possible combinations of input binary values alongside their corresponding output value. It helps logic designers analyze, define, verify, and simplify digital circuits and Boolean functions.

3. Explain the difference between analog and digital signals.

Answer:

- **Analog Signals:** Continuous signals that vary smoothly over time and can take an infinite number of intermediate voltage/amplitude values (e.g., human voice, temperature sensor output).
- **Digital Signals:** Discrete signals that represent data in distinct binary states (0 and 1or LOW and HIGH voltages), offering higher noise immunity and precision (e.g., computer clock signals).

4. Describe the function of a NOT gate with its truth table.

Answer: A NOT gate (or inverter) is a single-input, single-output logic gate that outputs the logical complement or inverse of its input. If the input is 0, the output is 1; if the input is 1, the output is 0.

Truth Table:

Input (A)	**Output ($\bar{A}$)**
0	1
1	0

5. What is the purpose of a Karnaugh map in simplifying Boolean expressions?

Answer: A Karnaugh map (K-map) provides a visual geometric method to simplify complex Boolean expressions. By grouping adjacent cells containing 1s according to specific powers of 2, K-maps eliminate redundant variables and yield minimal Sum-of-Products (SOP) or Product-of-Sums (POS) expressions without requiring tedious algebraic manipulation.

Long Questions

1. Explain the usage of Boolean functions in computers.

Answer:

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- **Digital Circuit Design:** Computer hardware operates exclusively on digital logic levels. Boolean functions define how physical logic gates (AND, OR, NOT, NAND, NOR, XOR) are interconnected inside microprocessors, memory controllers, and field-programmable gate arrays (FPGAs).
- **Arithmetic and Logic Unit (ALU):** The ALU performs all arithmetic operations (addition, subtraction) and logical evaluations (AND, OR, NOT) using hardware implementations of Boolean expressions, such as adders, comparators, and multipliers.
- **Control Units and Multiplexers:** Directing data flow along system buses, decoding instruction opcodes, and routing control signals depend entirely on complex Boolean functions designed to select specific hardware pathways.
- **Software Conditionals and Algorithms:** Programming statements (like if, while, AND, OR, NOT) evaluate logical flags and conditional branches using Boolean logic.

2. Describe how to construct a truth table for a Boolean expression with an example.

Answer:

- **Steps to Construct a Truth Table:**
  1. Determine the number of input variables (n). The total number of rows will be 2^n.
  2. Write down all binary combinations for the inputs in systematic order.
  3. Break down the expression into smaller sub-expressions or operations.
  4. Evaluate each sub-expression column by column.
  5. Compute the final output value for each row.
- **Example:** Construct a truth table for $F(A, B) = A \cdot \bar{B} + B$.

Inputs ($n = 2 \rightarrow 4$ rows*)*:

A	B	$\bar{B}$	$A \cdot \bar{B}$	$F = A \cdot \bar{B} + B$
0	0	1	0	**0**
0	1	0	0	**1**
1	0	1	1	**1**
1	1	0	0	**1**

3. Describe the concept of duality in Boolean algebra and provide an example to illustrate it.

Answer:

- **Concept:** The Duality Principle states that any true Boolean identity or algebraic expression remains true if all AND ($\cdot$) operators are swapped with OR ($+$) operators, all OR operators are swapped with AND operators, and all constants 0and 1are swapped ($0 \leftrightarrow 1$), while leaving variables unchanged.
- **Example:**
  - Original Identity: $A + 1 = 1$
  - Dual Identity: Swap $+$with $\cdot$, and 1with $0 \rightarrow A \cdot 0 = 0$.
  - Both original and dual statements hold universally true in Boolean algebra.

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4. Compare and contrast half-adders and full-adders, including their truth tables, Boolean expressions, and circuit diagrams.

Answer:

- **Comparison:**
  - **Half-Adder:** Adds two single binary bits (A and B). It produces a Sum (S) and a Carry (C). It cannot take an incoming carry from a previous stage into account.
  - **Full-Adder:** Adds three single binary bits (A, B, and an incoming carry C_{in}). It produces a Sum (S) and an outgoing Carry (C_{out}).
- **Truth Tables:**

Half-Adder Truth Table:

A	B	**Sum (S)**	**Carry (C)**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full-Adder Truth Table:

A	B	C_{in}	**Sum (S)**	**Carry (C_{out})**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- **Boolean Expressions:**
  - **Half-Adder:**

$$S = A \oplus B$$

$$S = A \oplus B$$

$$C = A \cdot B$$

$$C = A \cdot B$$

  - **Full-Adder:**

$$S = A \oplus B \oplus C_{in}$$

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$$S = A \oplus B \oplus C_{in}$$
$$C_{out} = (A \cdot B) + \left(C_{in} \cdot (A \oplus B)\right)$$

$$C_{out} = (A \cdot B) + \left(C_{in} \cdot (A \oplus B)\right)$$

- **Circuit Diagrams:**
  - **Half-Adder Circuit:** Constructed using an **XOR gate** (for Sum S) and an **AND gate** (for Carry C) with inputs $A$and Bconnected in parallel.
  - **Full-Adder Circuit:** Constructed using **two Half-Adders** and an **OR gate**. The first half-adder adds $A$and B; its Sum output along with C_{in}feeds the second half-adder to yield S. The carry outputs from both half-adders enter the OR gate to form C_{out}.

5. How do Karnaugh maps simplify Boolean expressions? Provide a detailed example with steps.

Answer:

- **Simplification Mechanism:** K-maps arrange minterms in a 2D grid based on **Gray Code** sequence (where adjacent cells differ by only one bit). This physical adjacency groups terms where a variable appears in both complemented and uncomplemented forms ($X + \bar{X} = 1$), enabling the variable to be factored out and eliminated.
- **Detailed Example:** Simplify $F(A, B) = \bar{A}\bar{B} + \bar{A}B + A\bar{B}$.
  - *Step 1:* Construct a 2-variable K-map grid (A along rows, Balong columns).
  - *Step 2:* Fill 1s into cells corresponding to the minterms:
    - $\bar{A}\bar{B} \rightarrow$ cell $(0,0) = 1$
    - $\bar{A}B \rightarrow$ cell $(0,1) = 1$
    - $A\bar{B} \rightarrow$ cell $(1,0) = 1$
  - *Step 3:* Form adjacent groups of 1s in sizes of powers of 2 (2, 4, etc.):
    - Group 1 (Top row containing $\bar{A}\bar{B}$and $\bar{A}B$): Variable Bchanges (B and $\bar{B}$cancel out), leaving $\bar{A}$.
    - Group 2 (Left column containing $\bar{A}\bar{B}$and $A\bar{B}$): Variable Achanges (A and $\bar{A}$cancel out), leaving $\bar{B}$.
  - *Step 4:* Combine minimized group terms:

$$F(A, B) = \bar{A} + \bar{B}$$

$$F(A, B) = \bar{A} + \bar{B}$$

6. Design a 4-bit binary adder using both half-adders and full-adders. Explain each step with truth tables, Boolean expressions, and circuit diagrams.

Answer:

- **Design Steps:**

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1. A 4-bit binary adder adds two 4-bit numbers: $A = A_3A_2A_1A_0$and $B = B_3B_2B_1B_0$.
2. **Stage 0 (LSB):** Uses a **Half-Adder** (or a Full-Adder with $C_{in} = 0$) to add bits $A_0$and B_0, outputting Sum bit $S_0$and Carry C_1.
   - *Expression:* $S_0 = A_0 \oplus B_0$, $C_1 = A_0 \cdot B_0$.
3. **Stage 1:** Uses a **Full-Adder** to add A_1, B_1, and incoming carry C_1, outputting Sum bit $S_1$and Carry C_2.
4. **Stage 2:** Uses a **Full-Adder** to add A_2, B_2, and incoming carry C_2, outputting Sum bit $S_2$and Carry C_3.
5. **Stage 3 (MSB):** Uses a **Full-Adder** to add A_3, B_3, and incoming carry C_3, outputting Sum bit $S_3$and final Carry C_4.

- **Circuit Diagram:** A cascade of 4 stages connected sequentially, where the carry output (C_{out}) of each stage is wired directly into the carry input (C_{in}) of the next stage (Ripple Carry Adder).

7. Simplify the following Boolean function using Boolean algebra rules:

$$F(A,B) = A \cdot B + A \cdot \bar{B}$$

$$F(A,B) = A \cdot B + A \cdot \bar{B}$$

Solution:

Factoring out Ausing Distributive Law:

$$F(A,B) = A \cdot (B + \bar{B})$$

$$F(A,B) = A \cdot (B + \bar{B})$$

Since $B + \bar{B} = 1$(Complement Law):

$$F(A,B) = A \cdot 1$$

$$F(A,B) = A \cdot 1$$

Since $A \cdot 1 = A$(Identity Law):

$$F(A,B) = A$$

$$F(A,B) = A$$

8. Use De Morgan's laws to simplify the following function:

$$F(A,B,C) = A + B + A \cdot C$$

$$F(A,B,C) = \overline{A + B + A \cdot C}$$

Solution:

Applying De Morgan's First Law ($\overline{X + Y + Z} = \bar{X} \cdot \bar{Y} \cdot \bar{Z}$):

$$F(A,B,C) = \bar{A} \cdot \bar{B} \cdot (A \cdot C)$$

$$F(A,B,C) = \bar{A} \cdot \bar{B} \cdot \overline{(A \cdot C)}$$

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Applying De Morgan's Second Law to $\overline{(A \cdot C)} = (\bar{A} + \bar{C})$:

$$F(A, B, C) = \bar{A} \cdot \bar{B} \cdot (\bar{A} + \bar{C})$$

$$F(A, B, C) = \bar{A} \cdot \bar{B} \cdot (\bar{A} + \bar{C})$$

Distributing $\bar{A} \cdot \bar{B}$inside the bracket:

$$F(A, B, C) = (\bar{A} \cdot \bar{B} \cdot \bar{A}) + (\bar{A} \cdot \bar{B} \cdot \bar{C})$$

$$F(A, B, C) = (\bar{A} \cdot \bar{B} \cdot \bar{A}) + (\bar{A} \cdot \bar{B} \cdot \bar{C})$$

Since $\bar{A} \cdot \bar{A} = \bar{A}$(Idempotent Law):

$$F(A, B, C) = (\bar{A} \cdot \bar{B}) + (\bar{A} \cdot \bar{B} \cdot \bar{C})$$

$$F(A, B, C) = (\bar{A} \cdot \bar{B}) + (\bar{A} \cdot \bar{B} \cdot \bar{C})$$

Factoring out $(\bar{A} \cdot \bar{B})$using Absorption Law $(X + X \cdot Y = X)$:

$$F(A, B, C) = \bar{A} \cdot \bar{B} \cdot (1 + \bar{C})$$

$$F(A, B, C) = \bar{A} \cdot \bar{B} \cdot (1 + \bar{C})$$

Since $1 + \bar{C} = 1$:

$$F(A, B, C) = \bar{A} \cdot \bar{B}$$

$$F(A, B, C) = \bar{A} \cdot \bar{B}$$

9. Simplify the following expressions:

- **(a)** $(A + \bar{B}) \cdot (A + B)$**:**

Applying Distributive Law $((X + Y)(X + Z) = X + Y \cdot Z)$:

$$= A + (\bar{B} \cdot B)$$

$$= A + (\bar{B} \cdot B)$$

Since $\bar{B} \cdot B = 0$:

$$= A + 0 = A$$

$$= A + 0 = A$$

- **(b)** $(A + \bar{B}) \cdot (\bar{A} + B)$**:**

Expanding using FOIL method:

$$= (A \cdot \bar{A}) + (A \cdot B) + (\bar{B} \cdot \bar{A}) + (\bar{B} \cdot B)$$

$$= (A \cdot \bar{A}) + (A \cdot B) + (\bar{B} \cdot \bar{A}) + (\bar{B} \cdot B)$$

Since $A \cdot \bar{A} = 0$and $\bar{B} \cdot B = 0$:

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$$= 0 + A \cdot B + \bar{A} \cdot \bar{B} + 0 = A \cdot B + \bar{A} \cdot \bar{B}$$

$$= 0 + A \cdot B + \bar{A} \cdot \bar{B} + 0 = A \cdot B + \bar{A} \cdot \bar{B}$$

(Equivalently, the XNOR operation $A \odot B$).

- **(c)** $A + \bar{A} \cdot (\bar{B} + C)$**:**

Applying Distributive Law ($X + \bar{X} \cdot Y = X + Y$):

$$= A + (\bar{B} + C) = A + \bar{B} + C$$

$$= A + (\bar{B} + C) = A + \bar{B} + C$$

- **(d)** $A \cdot B + A \cdot B$**:**

Applying Idempotent Law ($X + X = X$):

$$= A \cdot B$$

$$= A \cdot B$$

- **(e)** $(A \cdot B) + (\bar{A} \cdot \bar{B})$**:**

This expression is already in its minimal Sum-of-Products (SOP) canonical form for the **XNOR** function.

$$= A \odot B \text{ or } A \cdot B + \bar{A} \cdot \bar{B}$$

$$= A \odot B \quad \text{or} \quad A \cdot B + \bar{A} \cdot \bar{B}$$

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